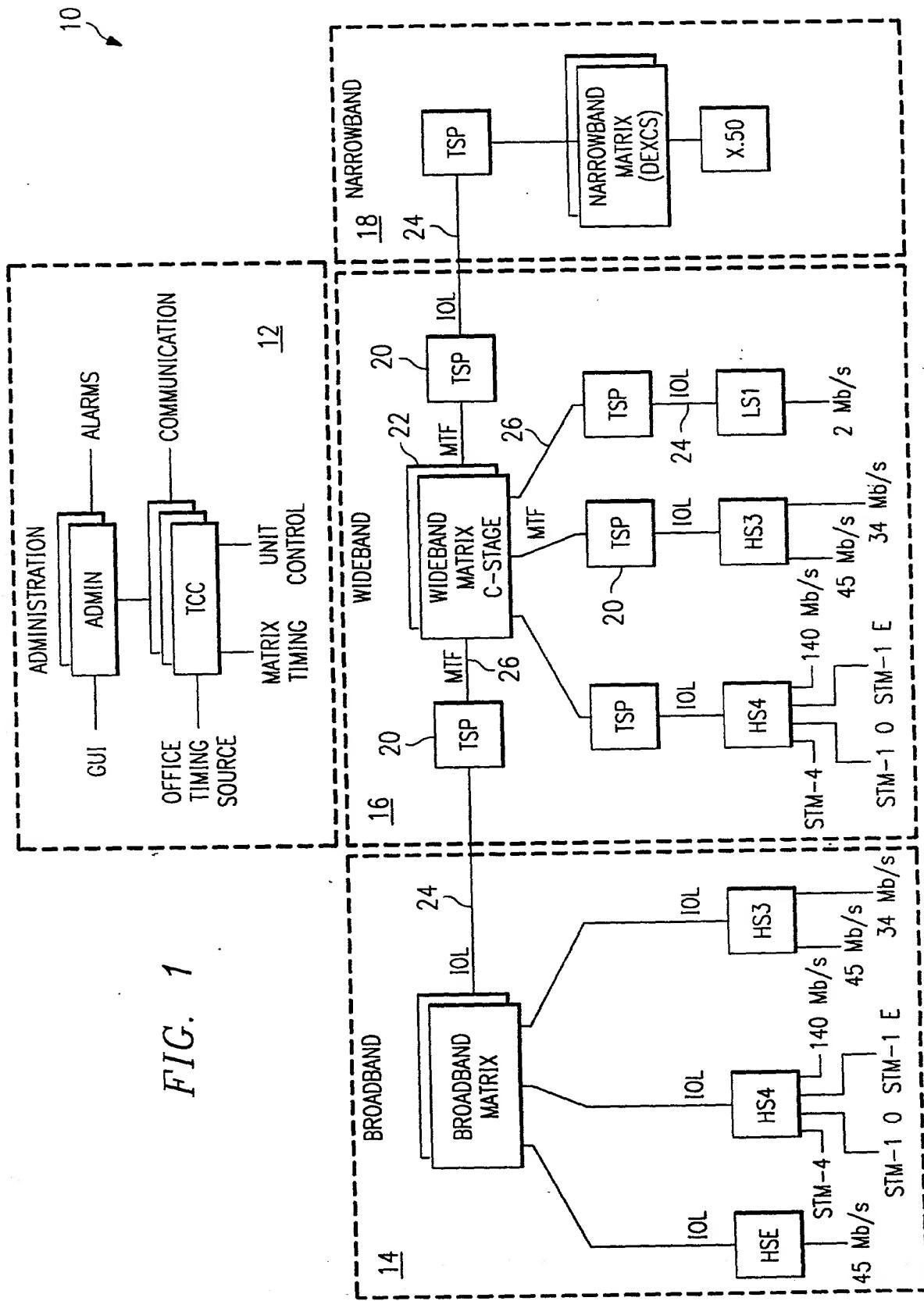


## PROCESSOR DEVICE FOR TERMINATING AND CREATING SYNCHRONOUS TRANSPORT SIGNALS

Inventors: Daniel P. Lyon, et al. Page 1 of 11  
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FIG. 1



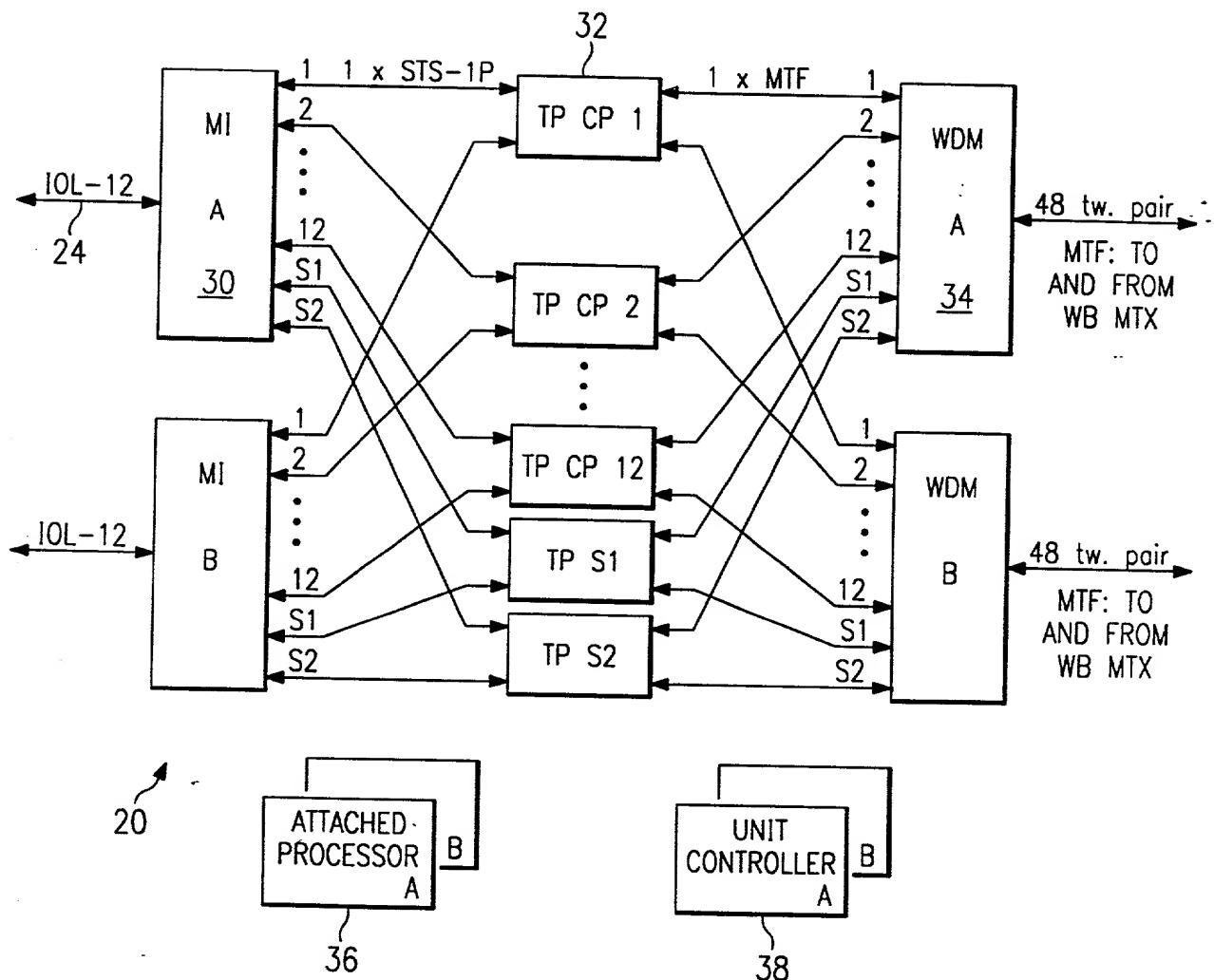
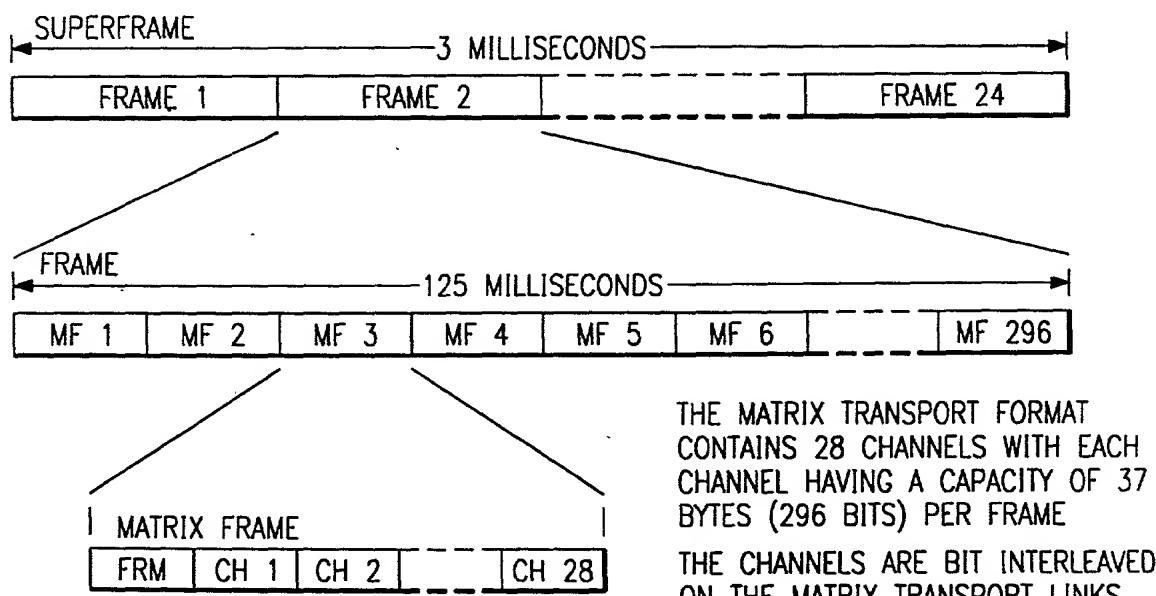


FIG. 2

	FRAME 1	FRAME 2	FRAME 3	FRAME 4
1	VTP (V1)	COH (V2)	R/P (V3)	R/P (V4)
2	78	R (V5)	26	52
3	79	1	27	53
4	80	2	28	54
5	81	3	29	55
6	82	4	30	56
7	83	5	31	57
8	84	6	32	58
9	85	7	33	59
10	86	8	34	60
11	87	9	35	61
12	88	10	36	62
13	89	11	37	63
14	90	12	38	64
15	91	13	39	65
16	92	14	40	66
17	93	15	41	67
18	94	16	42	68
19	95	17	43	69
20	96	18	44	70
21	97	19	45	71
22	98	20	46	72
23	99	21	47	73
24	100	22	48	74
25	101	23	49	75
26	102	24	50	76
27	103	25	51	77

COH - CHANNEL OVERHEAD  
VTP - VT PARITY  
R - RESERVED

FIG. 3



THE MATRIX TRANSPORT FORMAT  
CONTAINS 28 CHANNELS WITH EACH  
CHANNEL HAVING A CAPACITY OF 37  
BYTES (296 BITS) PER FRAME

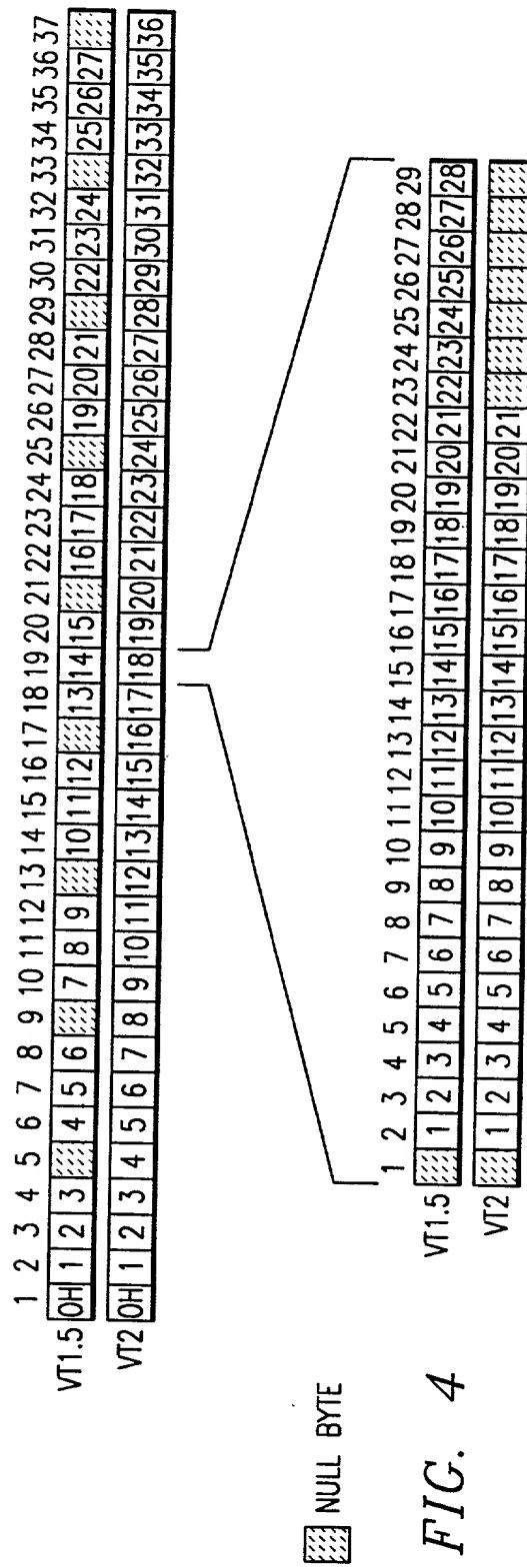
THE CHANNELS ARE BIT INTERLEAVED  
ON THE MATRIX TRANSPORT LINKS

MF X - MATRIX FRAME X

CH X - CHANNEL X BIT POSITION

MF FRM CODE - 0111

FIG. 5



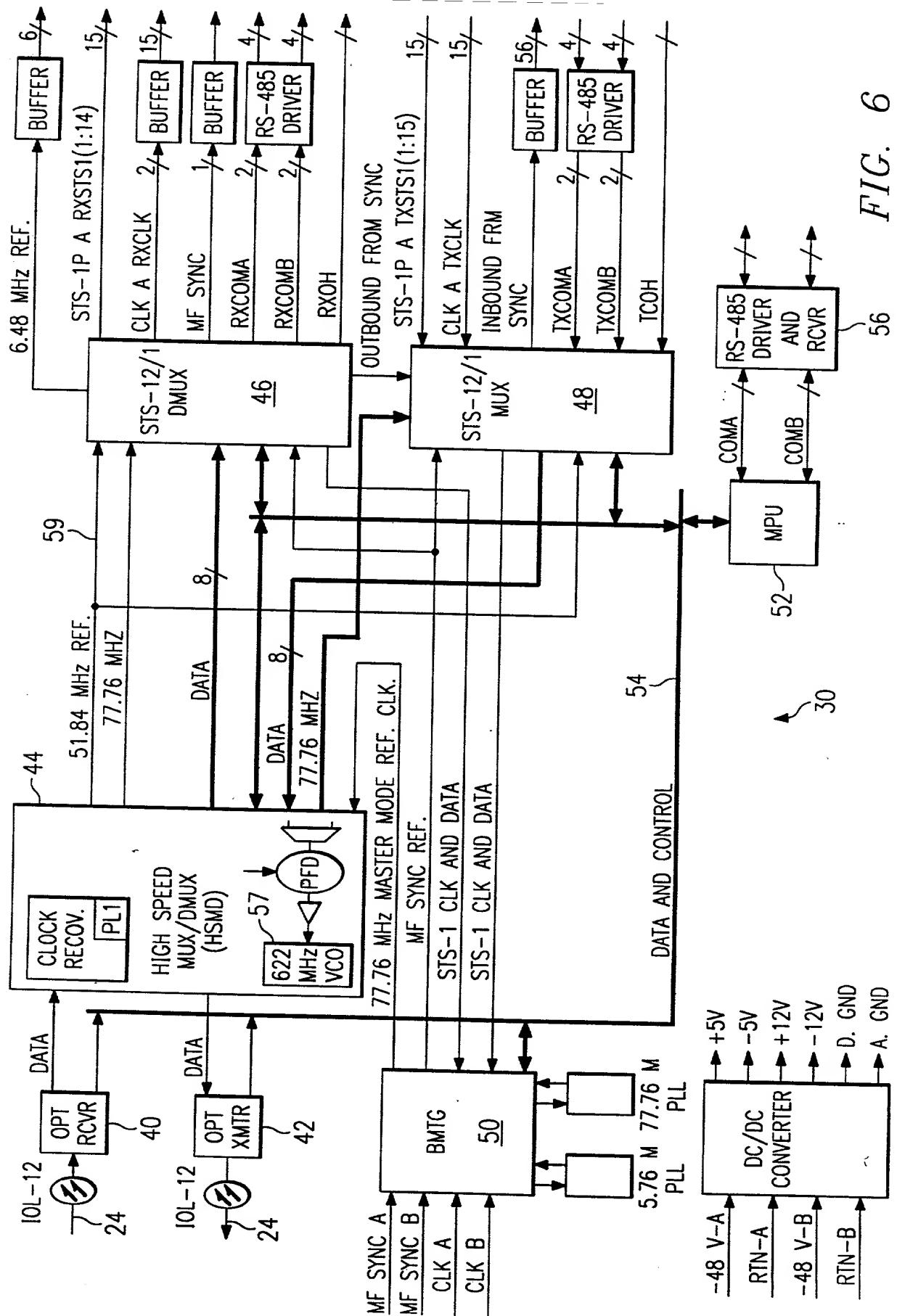
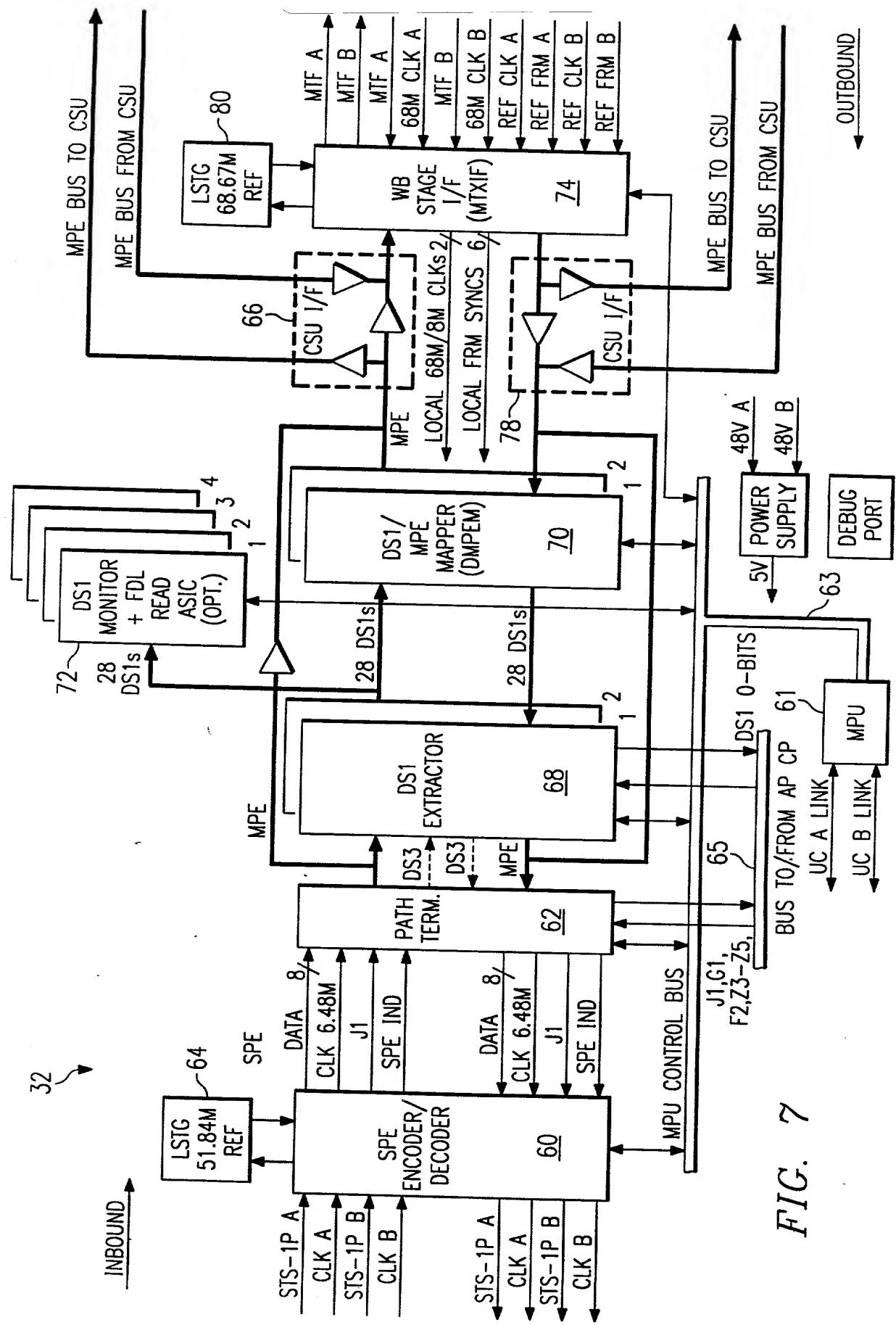


FIG. 6



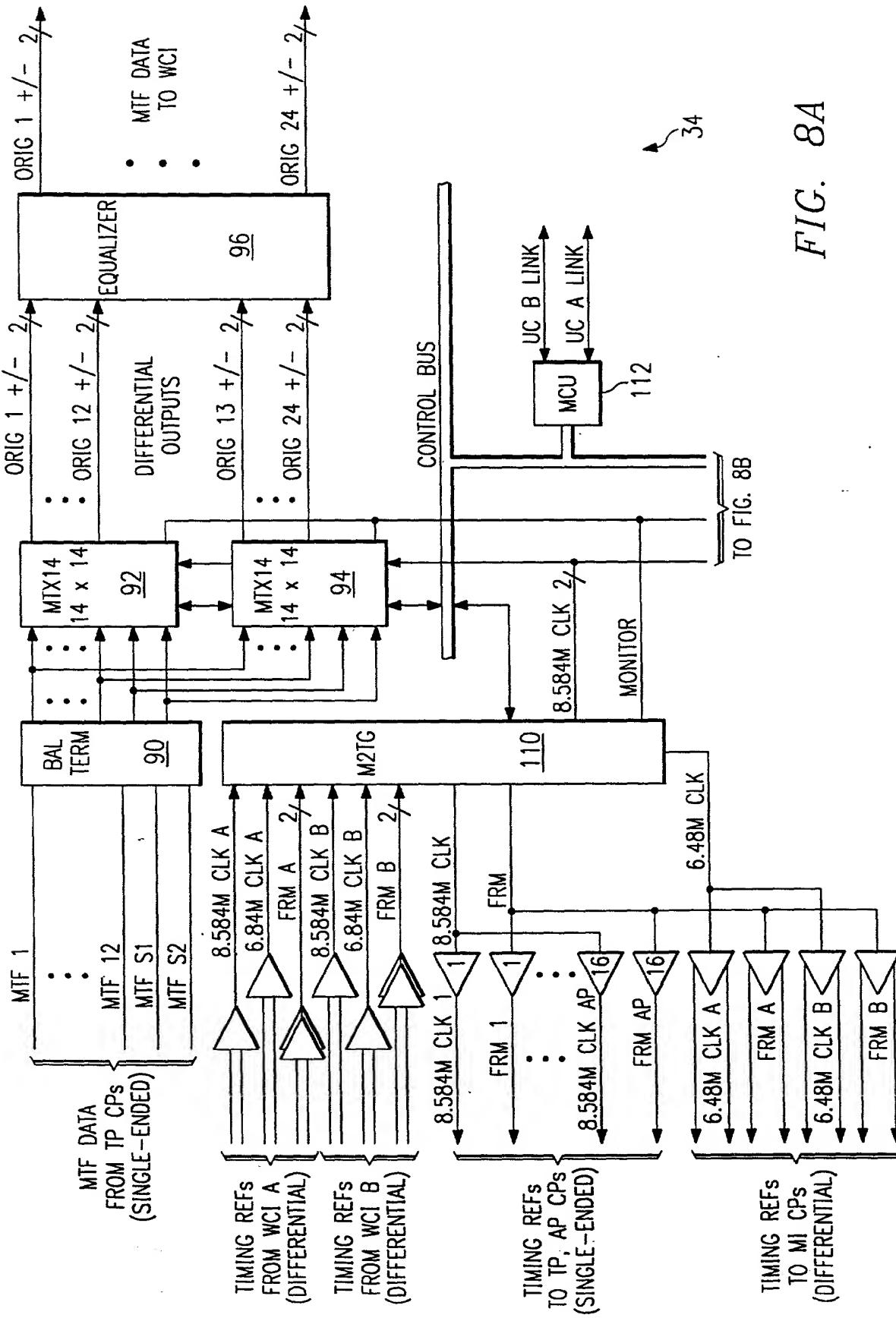
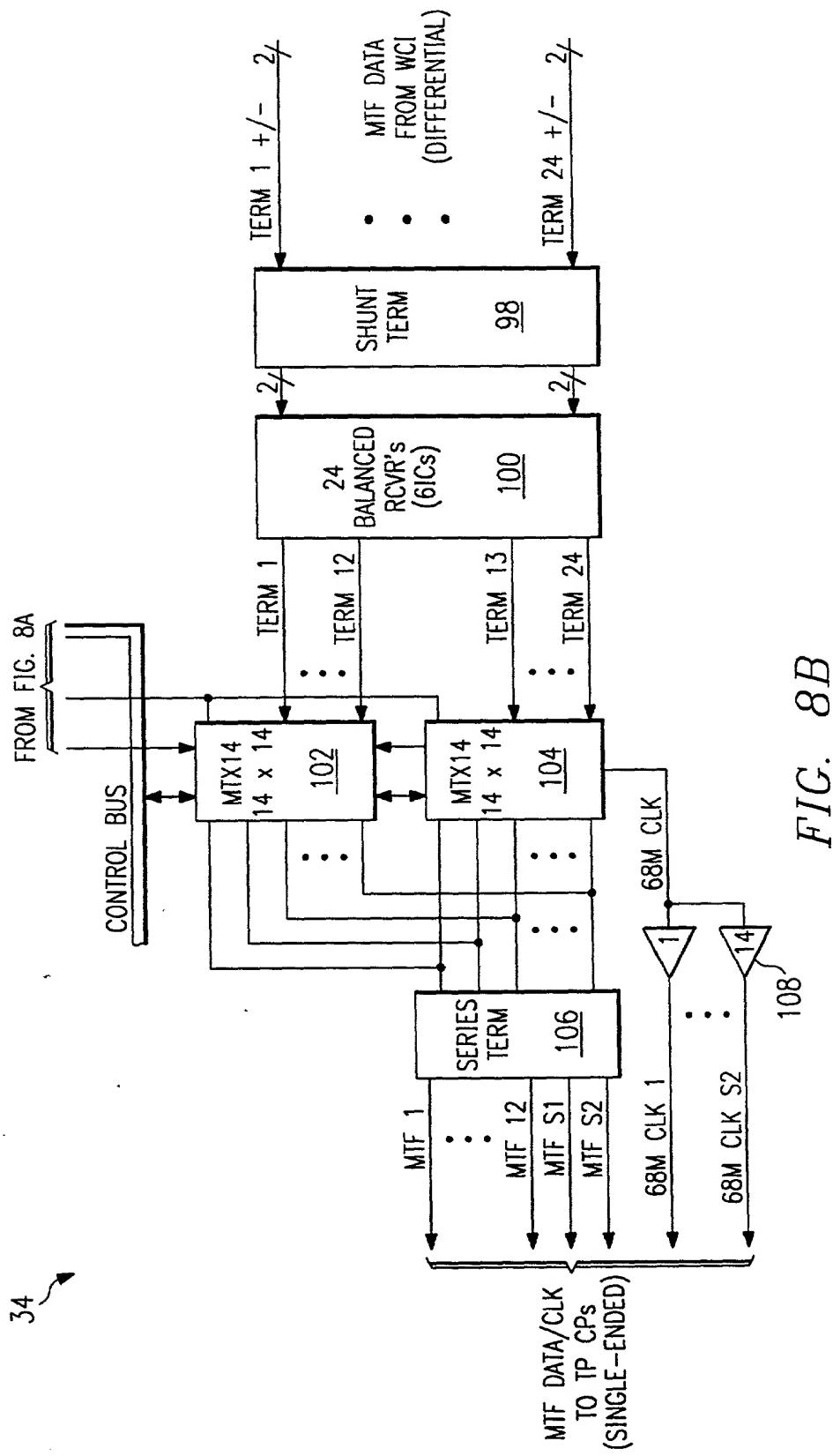


FIG. 8A



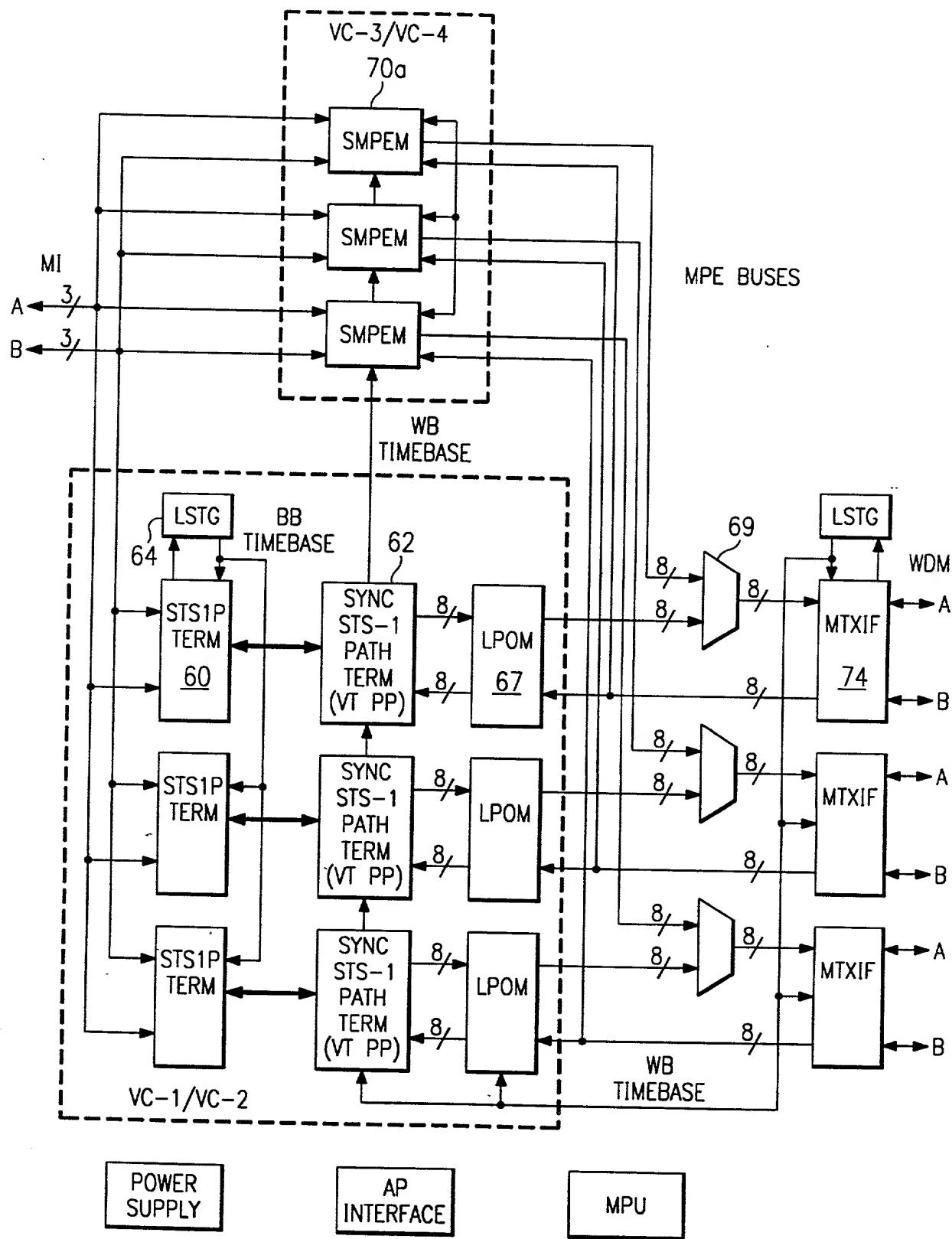


FIG. 9

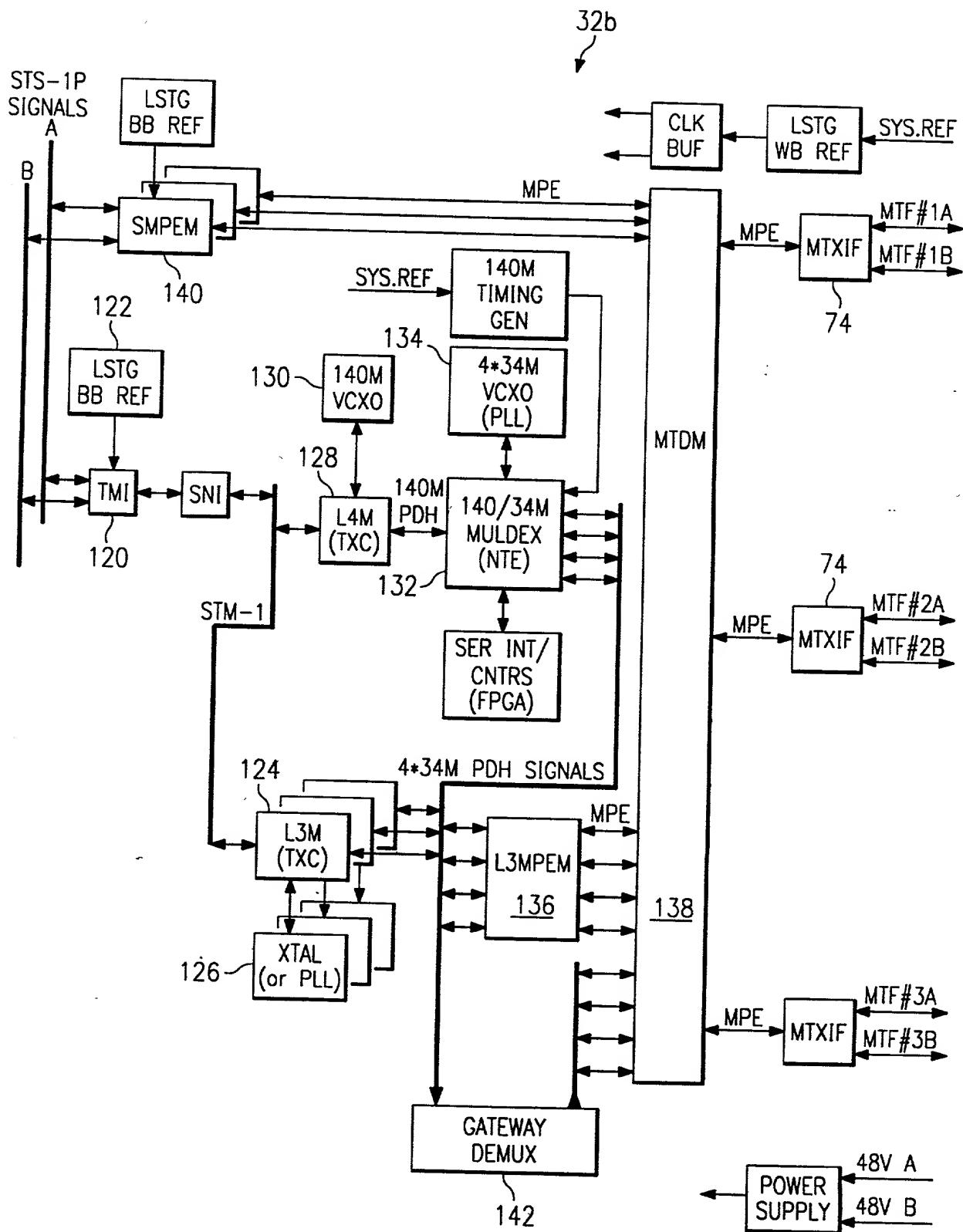


FIG. 10

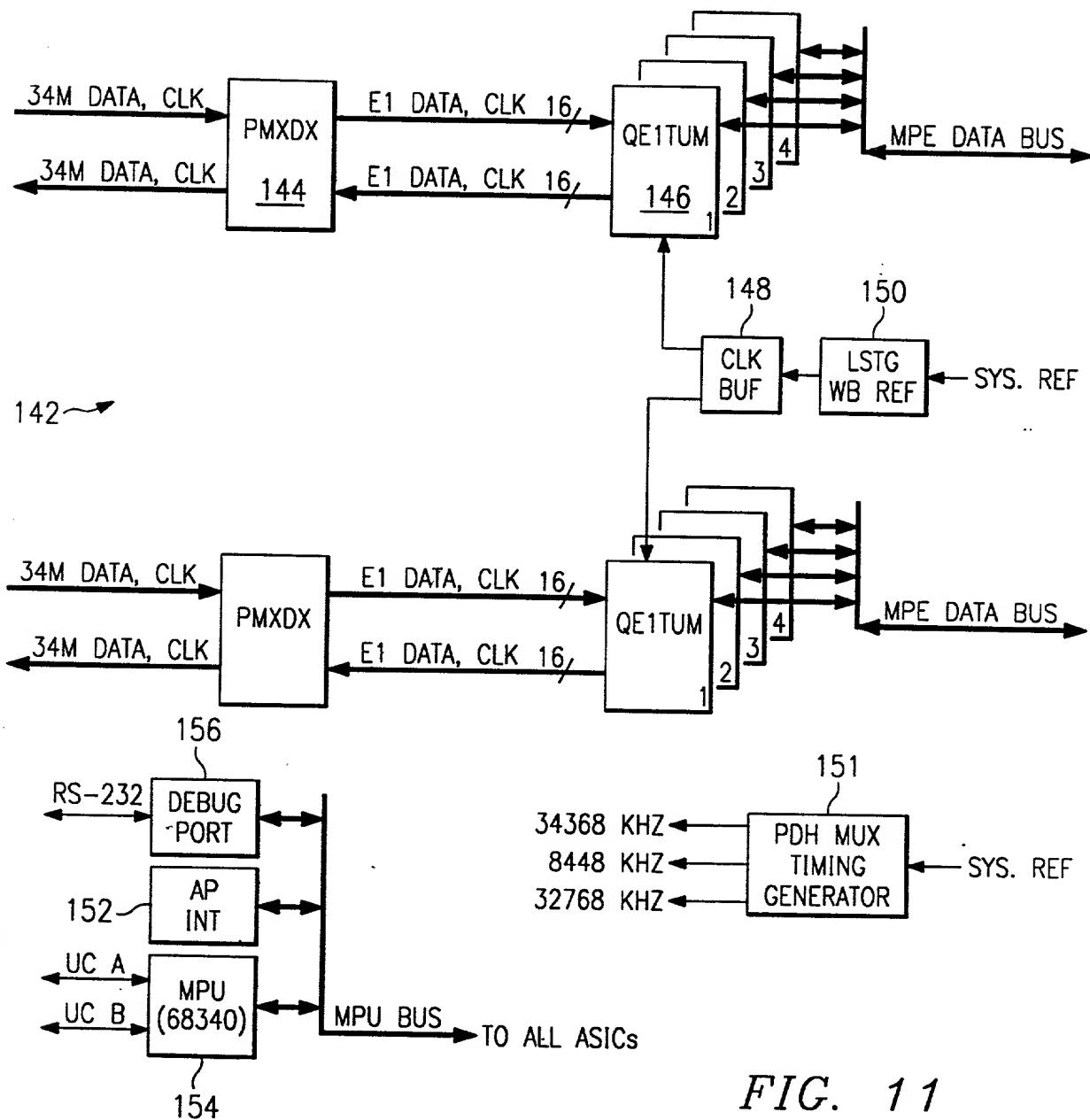


FIG. 11